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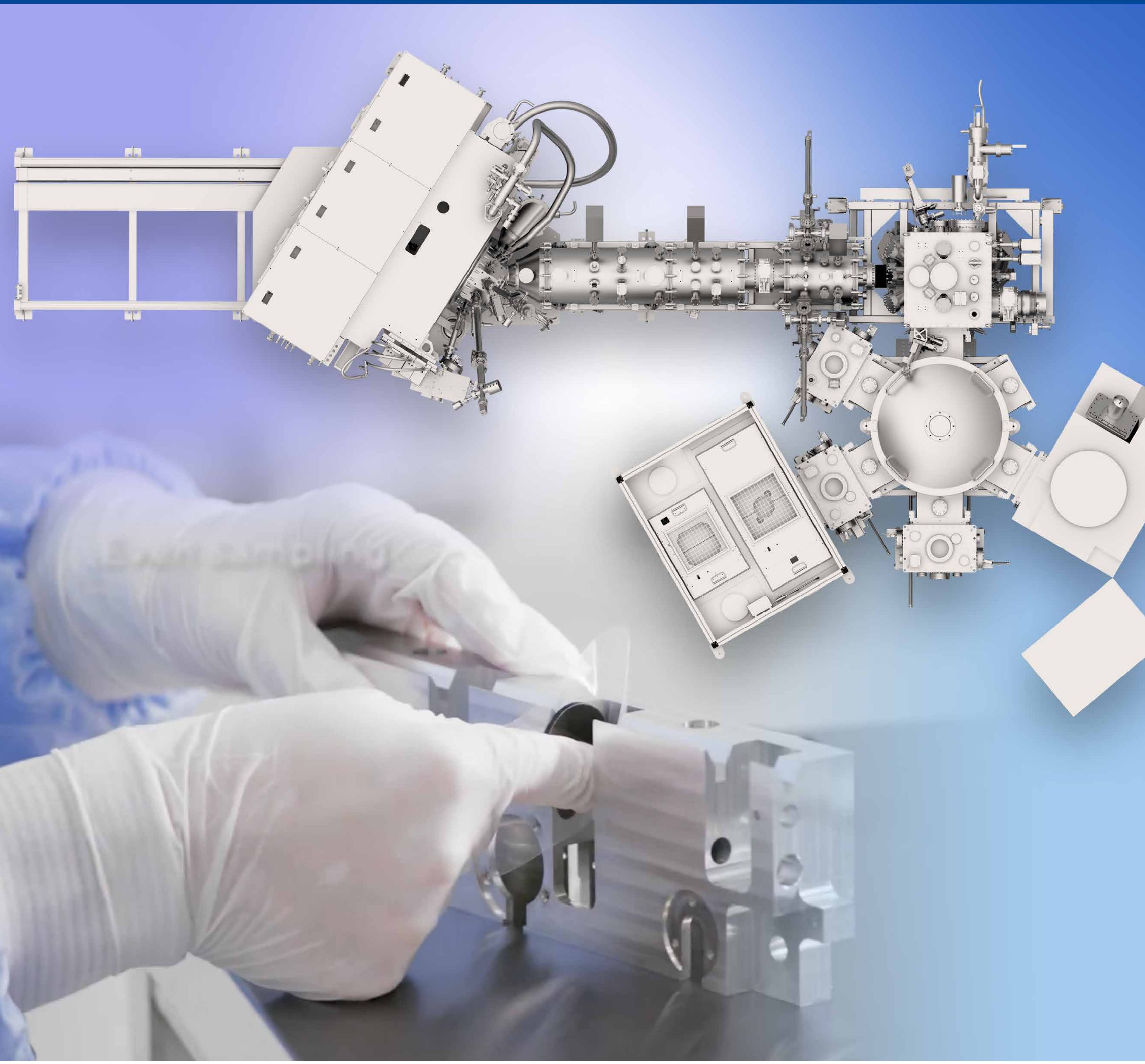

- THEME: CONTAMINATION
- GAS BEARING WORKSHOP 2021 REPORT
- THERMAL DESIGN FOR SOURCE OF MEDICAL RADIOISOTOPES
- PRECISION FAIR 2021 REPORT – THE FUTURE OF PRECISION ENGINEERING

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DSPE
YOUR PRECISION PORTAL

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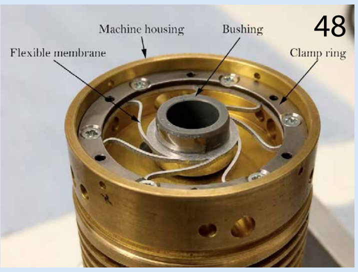
The cover illustration combines a photo of taking a sample for measuring contamination (lower left, courtesy Fastmicro) and a drawing of the EBL2 research facility (courtesy TNO). See pages 19 ff. and 31 ff.

IN THIS ISSUE

THEME: CONTAMINATION



FEATURES

DSPE UPDATE

Last month, the Precision Fair took place on 10 and 11 November. Luckily, the event could be organised in the Brabanthallen in Den Bosch (NL), which offered the fair a spacious environment to ensure maximum safety with respect to Covid-19. It was great to meet people face-to-face after almost two years of limited physical contacts. From our DSPE perspective, the two award ceremonies were among the highlights of the fair.

The Wim van der Hoek Award for the best master's thesis in the field of precision engineering was presented to Nick Habraken, who graduated from Eindhoven University of Technology on the redesign of a robot for microsurgery. Kees Verbaan earned the Ir. A. Davidson Award as an acknowledgement for his work as a system architect at first-tier system supplier NTS in Eindhoven (NL). In his position, he focuses on design challenges related to accurate positioning in complex machines. For the entire precision engineering community, it was, as always, a pleasure to put these award winners, and the six other nominees for the Wim van der Hoek Award, in the limelight.

At the fair, the annual general meeting offered us an excellent opportunity for updating the members on DSPE affairs. Julie van Stiphout, working as our office manager since February 2020, was introduced and the monthly online DSPE lunch meetings were reviewed; many thanks to the people from MI-Partners for coordinating the hosting of these meetings. Also, this year, the DSPE website has been refreshed with an appealing look & feel and a clear structure that is ready for adding new functionality.

Covid-19 has hampered knowledge sharing, but we hope to get back on track. Avoiding contamination has been a growing issue in the past decades, with the ongoing shrinkage of IC patterns in the semiconductor industry. Other industries also have a growing need for contamination control. DSPE is helping precision engineers to obtain more knowledge about this subject. This *Mikroniek* issue is dedicated to contamination control and last month a new knowledge day on contamination control has been organised.

A new edition of the DSPE Optics Week is under construction in collaboration with the German photonics network Optence. Our underlying goal with this week is to promote Dutch-German collaboration in the field of optics. The DSPE Optics Week consists of a one-day seminar and the three-day Optomechanical Systems Design course, which already has been successfully organised several times by DSPE.

Last but not least, DSPE wants to thank Hans van Eerden for his outstanding job in realising our great *Mikroniek* magazine.

Hans Krikhaar
President of DSPE and professor of Smart Manufacturing & Integrated Systems Engineering at Fontys University of Applied Sciences
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ACTIVE CONTAMINATION CONTROL FOR EQUIPMENT AND SUBSTRATES

High-end manufacturing equipment has to support increasing levels of cleanliness. First-tier high-tech system supplier VDL ETG is pro-actively developing capabilities in product design as well as in production process design to support increasing requirements on cleanliness. Where knowledge gaps exist, VDL ETG supports research to further the state-of-art, for example in the ACCESS project: Active Contamination Control for Equipment and SubstrateS. In this project, VDL ETG and Eindhoven University of Technology (TU/e) work together as a multidisciplinary team, to deepen the fundamental understanding of generation, transport and removal of particle contamination.

TON PEIJNENBURG , PAUL BLOM, LUUK BERKELAAR AND JAN-JAAP KONING

Introduction

With constantly increasing requirements on accuracy, productivity and yield, high-end manufacturing equipment has to support increasing levels of cleanliness. Sensitivity for particle, molecular and ionic contamination of advanced processes like semiconductor photolithography and electron microscopy increases with the capability for finer details and higher magnifications. The achievable cleanliness of equipment depends, on the one hand, on specific product design decisions and, on the other hand, on tight cleanliness control of parts manufacturing, assembly and integration processes.

As a tier-1 supplier to many high-end equipment OEMs in semiconductor, analytical, photonic and healthcare industries, VDL ETG, having its own design and engineering capabilities, is pro-actively developing capabilities in product design as well as in production process design to support increasing requirements on cleanliness. Where gaps in knowledge exist, VDL ETG will support research to further the state-of-art, in this case the ACCESS-project. ACCESS is the acronym for Active Contamination Control for Equipment and SubstrateS.

In the ACCESS-project, VDL ETG and various TU/e research groups work together as a multidisciplinary team, to deepen the fundamental understanding of generation, transport and removal of particle contamination. The scale of contamination affects processing of current- and next-generation semiconductor devices, and various kinds of analytical techniques such as electron microscopy, mass spectrometry and spectroscopy.

The project has been designed to be executed by 3 PhD students in combination with 6 PDEng (Professional Doctorate in Engineering) trainees, such that fundamental research activities can be combined with application-driven validation measurements and prototypes.

Background

With scaling continuing in different forms, e.g. shrink according to Moore's law, albeit currently at a reduced pace, and More-than-Moore initiatives such as multiscale packaging and 3D integration, the processes to manufacture semiconductor devices become more and more sensitive. The need for sufficient yield becomes more prominent with increasing sensitivity coupled to increased equipment cost. Also, more process steps become contamination-sensitive. Even more so, increasing the number of layers on a semiconductor wafer (like 3D NAND structures require), increases the susceptibility to contamination. In this highly demanding business environment, it is essential that equipment designers and equipment manufacturers develop deep understanding of particle (and other kinds of) contamination to guarantee sufficient cleanliness and sufficient yield of the production process.

Higher cleanliness reduces the sensitivity for contaminants. Contaminants can be divided into several classes [1]:

1. Particles.
2. Metal ions.
3. Chemicals.
4. Airborne molecular contaminants (AMCs).

AUTHORS' NOTE

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In semiconductors, the presence of contaminants can cause three major defects:

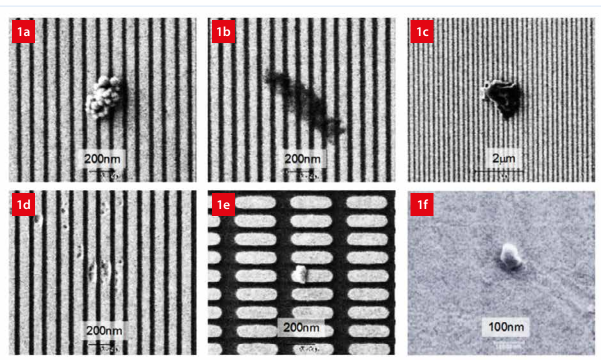
1. Device yield
   This is the most obvious defect and can easily be detected. Contaminants can cause the die to fail electrical tests and thus reduce yield.
2. Device performance
   Contamination can cause a lowering of device performance with time. This is a more serious problem because it causes lowering of device life.
3. Device reliability
   This is the hardest to detect because this can lead to failure, at some point in operational life.

Airborne contaminants (gases and particles) pose serious threats to high-tech industries with the critical dimension of e.g. a microelectronics chip quickly shrinking to nanoscale and the glass substrate of an LCD panel substantially growing to 1.9 m by 2.2 m. In theory, the best strategy to control the contaminants is to locate the emitting origin and to terminate the releasing source. The contaminants mainly originate from two sources: (a) incoming outdoor air, and (b) internal activities (Figure 1). Contamination is the main cause of a killer defect, that is any particle or any crystal defect that causes a disruption in an intended microcircuit pattern

The mechanism of contamination, e.g. in a semiconductor manufacturing environment [3]:

1. The source of contamination.
2. The transportation of the contamination.
3. The location of the contamination: surface, bulk.
4. The evolution of the contamination: how to remove it? Does the cleaning remove the contamination?

In semiconductor equipment, allowed contamination levels depend on productivity. Particle contamination characteristics for high-productivity lithographic equipment



Examples of surface contamination; the common defects induced by post-cleaning [2].
(a) Slurry abrasive particle remains.
(b) Organic residue.
(c) Polisher debris.
(d) Corrosion.
(e) Dendrites.
(f) Small residue defects.

Table 1
Progress over time in particle contamination characteristics for high-productivity lithographic equipment, in terms of particles per wafer pass (PWP) / size.

PWP / size	2015	2018	2022
wafer topside	0.5 / > 60 nm	0.5 / > 40 nm	0.05 / > 20 nm
wafer backside	2,500 / > 0.5 μm	1,750 / > 0.5 μm	600 / > 0.5 μm

are shown in Table 1. For metrology tools in a semiconductor manufacturing environment, having a lower productivity, a lower achievable PWP (particles per wafer pass) has been demonstrated by VDL ETG; 0.08 PWP / > 60 nm. Future requirements, in the next decade, however will even be stricter.

In scientific and analytical equipment, where high electric field strengths are used to generate an image (e.g. the optical path in electron optics), a single particle on a critical location already severely disturbs the image quality due to charging and arcing effects. When higher electric field strengths are implemented, the susceptibility to particle contamination even gets more critical.

Research approach

The purpose of the ACCESS project is to deepen our fundamental understanding of the (1) generation, (2) transport, and (3) removal of particle contamination. The scale of contamination affects processing of current- and next-generation semiconductor devices, and various kinds of analytical techniques such as electron microscopy, mass spectrometry and spectroscopy.

The work in the ACCESS research projects (see also the following articles) is carried out by three PhD students in various TU/e research groups, namely:

(1) Research project 1: Particle generation
    Research group: Mechanics of Materials (Mechanical Engineering department)
(2) Research project 2: Particle transport
    Research group: Turbulence and Vortex Dynamics (Applied Physics department)
(3) Research project 3: Particle cleaning
    Research group: Elementary Processes in Gas Discharges (Applied Physics department)

Each of the PhD students is assisted by two PDEng trainees to design and build experimental validation tools and prototypes. One of the PDEng trainees works in the Electrical Energy Systems research group at the TU/e Electrical Engineering department. The PhD students and the PDEng trainees are supervised by a technical project leader at the TU/e High Tech System

PRODUCT CLEANLINESS

In various industries there is an increasing need for guidance on nano- and microscale surface cleanliness for product development, part manufacturing, surface treatment, assembly, cleanliness measurements and cleanroom services. A VCCN project group therefore prepared the VCCN Guideline 12: Product Cleanliness. It does not prescribe solutions but describes what should be considered when dealing with product cleanliness, which should, among other things, enable and align the communication on product cleanliness between suppliers and customers, in order to help industries to realise and improve product cleanliness.

KOOS AGRICOLA

Cleanliness of product (or part) surfaces is important in many industries, such as aerospace, automotive, microelectronics, semiconductors, optics, nuclear, medical devices and life-science products. Surface cleanliness involves topics such as surface properties, manufacturing, cleaning, measures to keep a product clean during assembly, storage and transport, and measurements. Depending on the desired cleanliness of the product surface (with respect to particle and/or chemical concentrations), stringent methods must be used in the production flow to reach the cleanliness specifications. The product design should enable the realisation of a clean product. In case of application in high and ultrahigh vacuum (HV and UHV), additionally the selection of raw materials and the design of the part can influence the outgassing of the part.

Overview

VCCN guidelines are associated with international cleanroom standards prepared and published by the technical committees ISO TC 209 (Cleanrooms and associated controlled environments) and CEN TC 243 (Cleanroom technology). They provide additional information on cleanroom technology and contamination or cleanliness control. The recently published VCCN Guideline 12 (Figure 1) describes surface cleanliness of parts and products with respect to particles and chemicals. For some applications (especially in UHV) the emission of vapours caused by chemical contamination is of interest (RL 12 Product Cleanliness - VCCN) [1].
For the specification, realisation and verification of surface cleanliness it is crucial to understand the functions and application of the product. This motivates the product cleanliness requirements. During manufacturing, from raw material to delivered specified part or assembled device, the required surface cleanliness should be achieved. In general, the design is the starting point, but to be able to design a clean product, product developers should have knowledge of all cleanliness aspects. Various aspects have impact on the product cleanliness (see Figure 2).

AUTHOR'S NOTE

Koos Agricola is an applied physicist with 35 years' experience in contamination control and cleanroom technology. He is product manager and contamination control specialist at the Brookhuis Applied Data Intelligence cleanroom division in Enschede (NL). In addition, he is active in education and various (international) societies, including VCCN, and technical committees, covering standards for cleanroom technology and other topics in this field.

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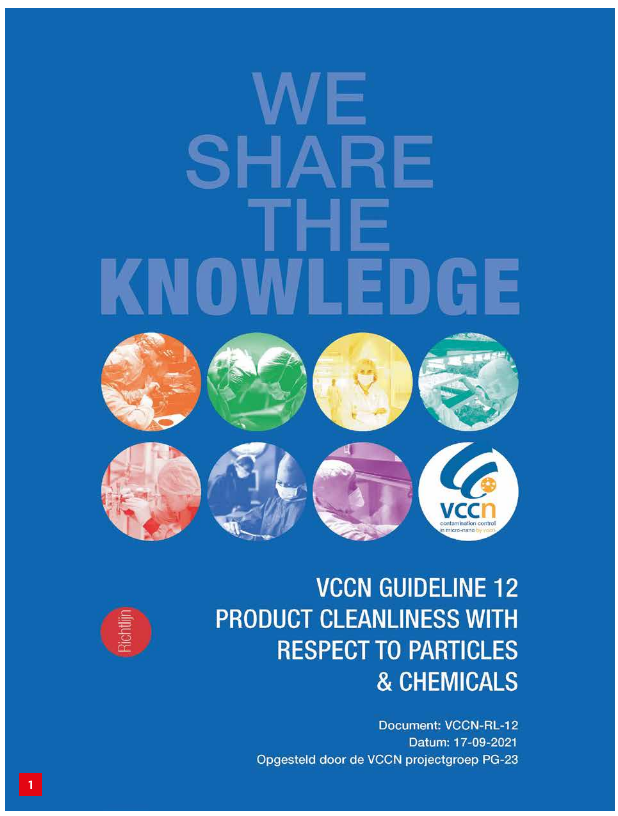
The following international standards on surface cleanliness are used [2]:

ISO 14644-9	Classification of surface cleanliness by particle concentration on surfaces, SCP.
ISO 14644-10	Classification of surface cleanliness by chemical concentration on surfaces, SCC.
ISO 14644-13	Cleaning of surfaces to achieve defined levels of cleanliness in terms of particle and chemical classifications.

Microbiological contamination topics are not specifically covered in the guideline, but various aspects such as design for cleanliness, specifications, assembly activities and controlled environments are also relevant for micro-



Cover of the recently published VCCN Guideline 12 document.

organisms. Their behaviour is comparable to that of particles (deposition, contact transfer) and molecular contamination (airborne transport of viruses), with the major deviations being the potential growth of micro-organisms and need for disinfection methods.
To achieve clean controlled environments, the following standards on air cleanliness with respect to particles and chemical concentrations can be used:

ISO 14644-1	Classification of cleanrooms.
ISO 14644-2	Monitoring air cleanliness with respect to particle concentration.
ISO 14644-8	Monitoring air cleanliness with respect to chemical concentration.

Additionally, ISO 14644 provides standards on cleaning, design, construction and start-up of cleanrooms, separative devices, as well as suitability of materials, consumables and equipment with respect to particle and chemical emission. For control of micro-organisms the use of EN17141:2020 "Biocontamination" is recommended [3].

VCCN Guideline 12 provides guidance on the major aspects of cleanliness of solid surfaces of parts, products, tools and equipment. The purpose is to align the communication between customer and supplier, on surface cleanliness specification and qualification and to provide guidance on means to reach and maintain specific cleanliness levels.

Surface cleanliness involves the determination, reduction and prevention of contamination by particles and/or chemical compounds and/or trace elements. Important aspects are:

- Specification: Expression of the required level of surface cleanliness with respect to particles and chemicals.
- Measurement: Determination of the level of surface cleanliness with respect to particles and chemicals as can be used in qualification and monitoring.
- Raw materials: Impact on surface cleanliness and outgassing behaviour.
- Manufacturing: Process conditions and part treatment during manufacturing with respect to surface cleanliness.
- Cleaning: Selection and evaluation of methods for cleaning to a specified degree of surface cleanliness.
- Assembly: Maintaining initial surface cleanliness by proper environmental cleanliness, operational procedures and working methods.
- Packaging: Impact of packaging on the surface cleanliness of solid surfaces.
- Design: Aspects that have impact on the achievable surface cleanliness and cleaning.

Surface cleanliness starts with the specification of the customer demands. During this phase, the requirements are set that must be met during a chain of activities. A typical chain of activities is shown in the process flow in Figure 3. The process flow of the manufacturing of a clean product starts with the specification of the raw material and ends with the delivery of a specified part or assembled device to the customer.

For specification of surface cleanliness, product functions and types of contamination that can harm the function or application of a part (or the function of the device in which the part is used) must be described. The contamination can consist of specific particles and/or chemicals. Particulate contamination can cause electric opens or shorts, geometric defects, obscuration and (micro)mechanical defects. Chemical contamination can cause unacceptable off-gassing or outgassing of a product and unacceptable chemical interactions, such as corrosion, and have an unacceptable negative impact on adhesion of coatings and adhesives, etc.

Surface cleanliness levels are expressed in contamination concentration (mass and particle area or number) per surface area. Levels are described according to the ISO standard or guideline the customer and supplier agree(d) to use. The next step is to select the appropriate measurement method(s). Preferably the surface cleanliness is specified with respect to the recommended measurement method.

Contamination control

The starting point of manufacturing is the raw material that is used to make a part. Composition, purity and structure will have impact on the achievable surface cleanliness. An important fabrication (material transformation) process is machining and this will have impact on the surface contamination and cleanability.

After transformation, a dirty or unclean surface needs to be cleaned to a specified surface cleanliness level. There are many cleaning methods that can be used to clean a part. The selection depends on the levels to be reached, type of contamination, the material and the acceptable level of damage by the cleaning process. For the selection of a cleaning method, the cleaning efficiency and/or effectivity of the cleaning method should be evaluated.

Clean parts can be contaminated during assembly of the product. Often, assembled surfaces cannot be cleaned afterwards. A risk assessment on the likelihood and consequences of contamination during product assembly will help to identify locations where contamination should be prevented. To limit and control unwanted contamination, a clean environment and specific operational measures are required. The complete set of measures to achieve